Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Previously Presented) A semiconductor device, comprising:

a dielectric layer;

an electrically conductive copper containing layer; and

a barrier layer, separating the dielectric layer from the copper containing layer, comprising a silicon oxide layer doped with divalent ion dopant, wherein a ratio of dopant ions to silicon oxide molecules adjacent to the copper layer is within the range from 1:2 to 1:6.

2. (Original) The semiconductor device, as recited in claim 1, wherein the dopant is selected from the group containing beryllium, magnesium, calcium, strontium, and barium.

3. (Original) The semiconductor device, as recited in claim 1, wherein the dopant is calcium.

4. (Canceled)

5. (Original) The semiconductor device, as recited in claim 3, wherein a ratio of calcium ions to silicon oxide molecules adjacent to the copper layer is within the range from 1:3 to 1:4.

6. (Previously Presented) The semiconductor device, as recited in claim 3, wherein at least about 98% of the calcium dopant is within the silicon oxide in a region that extends from a surface of the barrier layer adjacent to the copper containing layer to a depth of less than about 340 Å.

7. (Previously Presented) The semiconductor device, as recited in claim 3, wherein at least about 98% of the calcium dopant is within the silicon oxide in a region that extends from a surface of the barrier layer adjacent to the copper containing layer to a depth of less than about 170 Å.

8. (Original) The semiconductor device, as recited in claim 6, wherein the barrier layer is a first barrier layer on a first side of the copper containing layer, and further comprising a second barrier layer on a second side of the copper containing layer, wherein the second barrier layer comprises:

silicon oxide; and

a dopant, wherein the dopant is a divalent ion, which dopes the silicon oxide adjacent to the copper containing layer.

9. (Canceled)

10. (Original) The semiconductor device, as recited in claim 1, wherein a ratio of dopant ions to silicon oxide molecules adjacent to the copper layer is within the range from 1:3 to 1:4.

11. (Previously Presented) A semiconductor device comprising:

a dielectric layer;

an electrically conductive copper containing layer; and

a barrier layer, separating the dielectric layer from the copper containing layer, comprising a silicon oxide layer doped with divalent ion dopant, wherein at least about 98% of the dopant is within the silicon oxide in a region that extends from a surface of the barrier layer adjacent to the copper containing layer to a depth of less than about 340 Å.

12. (Previously Presented) A semiconductor device comprising:

a dielectric layer;

an electrically conductive copper containing layer; and

a barrier layer, separating the dielectric layer from the copper containing layer, comprising a silicon oxide layer doped with divalent ion dopant, wherein at least about 98% of the dopant is within the silicon oxide in a region that extends from a surface of the barrier layer adjacent to the copper containing layer to a depth of less than about 170 Å.

13. (Original) The semiconductor device, as recited in claim 1, wherein the barrier layer is a first barrier layer on a first side of the copper containing layer, and further comprising a second barrier layer on a second side of the copper containing layer, wherein the second barrier layer comprises:

silicon oxide; and

a dopant, wherein the dopant is a divalent ion, which dopes the silicon oxide adjacent to the copper containing layer.

14. (Canceled)

15. (Previously Presented) A method of forming a barrier layer, comprising:

providing a silicon oxide layer with a surface;

doping the surface of the silicon oxide layer with a divalent ion to form a barrier layer extending from within the silicon oxide layer to the surface of the silicon oxide layer;

forming an electrically conductive copper containing layer on the surface of the barrier layer, wherein the barrier layer prevents diffusion of copper into the substrate; and

annealing the barrier layer.

16. (Original) The method, as recited in claim 15, further comprising:

forming a second silicon oxide layer on a surface of the copper containing layer; and

doping the second silicon oxide layer with a divalent dopant to form a second barrier layer.

17. (Original) The method, as recited in claim 16, wherein the divalent dopant is selected from the group containing beryllium, magnesium, calcium, strontium, and barium.

18. (Previously Presented) A semiconductor device, comprising:

an electrically conductive copper containing layer; and

a barrier layer adjacent to the copper containing layer, comprising a silicon oxide layer doped with divalent ion dopant, wherein the dopant is implanted in the silicon oxide layer using at least one of ion implantation and plasma implantation.

19. (Original) The semiconductor device, as recited in claim 18, wherein the dopant is selected from the group containing beryllium, magnesium, calcium, strontium, and barium.

20. (Original) The semiconductor device, as recited in claim 18, wherein the dopant is calcium.

21. (Previously Presented) A method of forming a barrier layer, comprising:

providing a silicon oxide layer with a surface;

implanting divalent ions into the silicon oxide layer to form a barrier layer extending to the surface of the silicon oxide layer; and

forming an electrically conductive copper containing layer on the surface of the barrier layer, wherein the barrier layer prevents diffusion of copper into the substrate.

22. (Previously Presented) The method, as recited in claim 21, wherein the implanting comprises at least one of ion implantation and plasma implantation.